**In the Claims:**

1-13. (Canceled)

14. (Currently Amended) An integrated circuit ~~substrate Read Only Memory (ROM)~~ device, comprising:

an integrated circuit substrate including a planar face;

[[an]] a planar insulating layer [[on]] extending along the planar face of the integrated circuit substrate;

a first planar conductive layer pattern including a sidewall, [[on]] extending along the planar insulating layer opposite the planar face of the integrated circuit substrate;

a thermal oxide layer on the integrated circuit substrate and directly on the sidewall of the first planar conductive layer pattern;

a buried doping layer in the integrated circuit substrate beneath the thermal oxide layer; and

a second conductive layer pattern on at least a portion of the thermal oxide layer and on at least a portion of the first planar conductive layer pattern.

15. (Currently Amended) A [[ROM]] device according to Claim 14 wherein the second conductive layer pattern is directly on the first planar conductive layer pattern opposite the planar insulating layer.

16. (Currently Amended) A [[ROM]] device according to Claim 14 wherein the first planar and second conductive layer patterns both comprise polysilicon.

17. (Currently Amended) A [[ROM]] device according to Claim 14 further comprising a read only memory programming region in the integrated circuit substrate beneath the planar insulating layer.

18. (Currently Amended) A device according to Claim 17 wherein the read only memory programming region comprises an implant region in the integrated circuit substrate beneath the planar insulating layer.

19. (Currently Amended) A [[ROM]] device according to Claim 14 wherein the second conductive layer pattern is not directly on the sidewall of the first planar conductive layer pattern.

20. (New) An integrated circuit substrate Read Only Memory (ROM) device, comprising:

an integrated circuit substrate;

an insulating layer on the integrated circuit substrate;

a ROM programming region in the integrated circuit substrate beneath the insulating layer;

a first conductive layer pattern including a sidewall, on the insulating layer opposite the integrated circuit substrate;

a thermal oxide layer on the integrated circuit substrate and directly on the sidewall of the first conductive layer pattern;

a buried doping layer in the integrated circuit substrate beneath the thermal oxide layer; and

a second conductive layer pattern on at least a portion of the thermal oxide layer and on at least a portion of the first conductive layer pattern.

21. (New) A ROM device according to Claim 20 wherein the second conductive layer pattern is directly on the first conductive layer pattern opposite the insulating layer.

22. (New) A ROM device according to Claim 20 wherein the first and second conductive layer patterns both comprise polysilicon.

23. (New) A ROM device according to Claim 20 wherein the ROM programming region comprises an implant region in the integrated circuit substrate beneath the insulating layer.

24. (New) A ROM device according to Claim 20 wherein the second conductive layer pattern is not directly on the sidewall of the first conductive layer pattern.